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EXAMINER	
YU, JAE UN	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,197	COHEN, ERNEST S.	
	Examiner	Art Unit	
	Jae U. Yu	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of the amendment dated 3/28/2006. At this point claims 1, 5, 6, 7, 10, 13, 14, 19 and 23 are amended. Thus, claims 1-24 are pending in the instant application.

Response to Amendment

In view of the applicant's amendment, the original rejections dated 12/29/2005 to claims 1-24 are withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-24 are rejected under 35 USC 103 (a) as being obvious over Harvey et al. (US 6,233,668) in view of Budd et al. (US 2003/0177435).

2. As per **independent claim 1**, Harvey et al. discloses, "a computer-readable medium having encoded thereon computer-executable instructions **["A storage medium containing instructions readable by a computer system", Column 22, Lines 54-58]**".

"For at least one of the plurality of page tables **["A page table", Column 4, Lines 1-3]**, creating a first shadow page table **["Self-mapping Page Tables" coinciding in virtual-address space, Column 4, Lines 1-3]** based on said one of the plurality of page tables".

"At least one entry in said first shadow page table links to a different data page **[Materialized in ("linked to") different "physical-address locations", Column 4, Lines 11-15]** than that entry's corresponding link **[Coinciding in virtual-address space, Column 4, Lines 11-15]** in said one of the plurality of page tables"

"Said first shadow table contains one or more read-only links **["Write-protected" subtable reference, Column 17, Lines 1-4]** whose corresponding links in said one of the plurality of page tables are read/write **["Write access" referring the subtable, Column 16, Lines 65-68]**"

"Creating a shadow page directory **[Element 96, Figure 3]** based on the page directory, the page directory comprising a link to said one of the plurality of page tables **["MLST" 78, Figure 3]**, said shadow page directory comprising a link to said shadow page table **["MLST" 80, Figure 3]** instead of the link to said one of said plurality of page tables"

Harvey et al. do not disclose expressly, "an item of software uses said page table to perform a non-address-mapping action that depends on data that a characteristic that

is present in said one of the plurality of page tables but not present in said first shadow page table".

Budd et al. disclose application software that performs a non-address-mapping action (comparing the stored "checksum" and the data) in paragraph 62.

Harvey et al. and Budd et al. are analogous art because they are from the same field of endeavor of memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Harvey et al. by including an application software that performs checksum calculation as taught by Budd et al. in paragraph 62.

The motivation for doing so would have been to detect the corruption before the actual I/O submission as expressly taught by Budd et al. in paragraph 62.

Therefore, it would have been obvious to combine Budd et al. with Harvey et al. for the benefit of early detection of data corruption to obtain the invention as specified in claim 1.

3. As per **independent claim 5**, Harvey et al. disclose, "a memory **["Memory" 14, Figure 1]** comprising a plurality of individually-addressable components that can be read and written **[Read and write memory access (Column 16, Line 63 – Column 17, Line 6)]**, each of the plurality of the individually-addressable components having a

physical address **["Physical-address Locations", Column 4, Lines 11-15]** associated therewith".

"An address translation data structure **[Figure 3]** that defines a mapping between virtual addresses **["Virtual Address", Figure 1]** and the physical addresses **["Physical Address", Figure 1]** of the individually-addressable components"

"A memory manager **["MMU" 20, Figure 1]** that receives a request to access a first one of the individually-addressable components, said request identifying said first one of the individually-addressable components based on a virtual address **["Virtual Address", Figure 1]**, said memory manager translating said virtual address into the physical address of said first one of the individually-accessible components **["Physical Address" for "Memory" 14, Figure 1]** based on data that comprises a shadow representation of said address translation data structure" **In column 9, at lines 25-28, Harvey et al. recites, "The subtables located at some virtual-memory locations have different versions for different processes, and each is therefore materialized in different physical memory."** There are multiple versions for the "subtables" (corresponding to the "shadow representation" from the claim), and they are "materialized" ("translated") to the "physical memory".

Harvey et al. do not disclose expressly, "an item of software that uses said address translation data structure to perform non-address-mapping action that depends

on data that has a characteristic that is present in said address translation structure but not present in said shadow representation of said address translation structure".

Budd et al. disclose application software that performs a non-address-mapping action (comparing the stored "checksum" and the data) in paragraph 62.

Harvey et al. and Budd et al. are analogous art because they are from the same field of endeavor of memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Harvey et al. by including an application software that performs checksum calculation as taught by Budd et al. in paragraph 62.

The motivation for doing so would have been to detect the corruption before the actual I/O submission as expressly taught by Budd et al. in paragraph 62.

Therefore, it would have been obvious to combine Budd et al. with Harvey et al. for the benefit of early detection of data corruption to obtain the invention as specified in claim 5.

4. As per **independent claim 14**, Harvey et al. disclose, "receiving an request to read or write a unit of a memory **[Receiving an request to access memory, Figure 1]**, said request identifying said unit of said memory based on a virtual address **["Virtual Address", Figure 1]**".

"Accessing said unit of memory based on a representation of a map **[Figure 3]** that defines a relationship between virtual addresses and physical addresses" **In column 5, at lines 30-33, Harvey et al. recites, "Each process is given a page table, whose entries indicate the physical location of "page frames" that contain respective virtual memory "pages"."**

"Said representation of said map comprising at least one shadow page **["Self-mapping Page Tables" coinciding in virtual-address space, Column 4, Lines 1-3]** that is based on a first one of said one or more pages **["A page table", Column 4, Lines 1-3]**"

"Said map including at least one aspect which, if used to access said memory based on said virtual address, would result in violation of a memory access policy, said shadow page differing from said first one of said one or more pages in a manner such that use of said representation of said map to access said memory based on said virtual address does not violate said memory access policy. Performing the read or write specified in said access request." **In column 15, at lines 13-16, Harvey et al. recites, "This exception handler has been arranged in the illustrated embodiment to determine whether a true access violation has actually occurred",** which corresponds to the "policy" from the claim. **In column 15, at lines 26-31, Harvey et al. recites, "The handler compares the faulting reference with the shared/physical boundary to determine which of the two physical page frames identified by FIG. 3's registers 38 and 122 is the one that properly contains the page translation for that**

reference, and it fetches the proper entry by physical addressing." The "faulting reference" corresponds to the "virtual address results in violation" from the claim, and "fetching the proper entry by physical addressing" corresponds to the "virtual address does not result in violation" from the claim.

Harvey et al. do not disclose expressly, "an item of software uses said page table to perform a non-address-mapping action that depends on data that a characteristic that is present in said one of the plurality of page tables but not present in said first shadow page table".

Budd et al. disclose application software that performs a non-address-mapping action (comparing the stored "checksum" and the data) in paragraph 62.

Harvey et al. and Budd et al. are analogous art because they are from the same field of endeavor of memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Harvey et al. by including an application software that performs checksum calculation as taught by Budd et al. in paragraph 62.

The motivation for doing so would have been to detect the corruption before the actual I/O submission as expressly taught by Budd et al. in paragraph 62.

Therefore, it would have been obvious to combine Budd et al. with Harvey et al. for the benefit of early detection of data corruption to obtain the invention as specified in claim 14.

5. As per **independent claim 19**, Harvey et al. discloses, "a shadow page table **["Self-mapping Page Tables" coinciding in virtual-address space, Column 4, Lines 1-3]** that is based on a first one of the plurality of page tables **["A page table", Column 4, Lines 1-3]**".

"A shadow page directory **[Element 96, Figure 3]** that is based on the page directory, the page directory comprising a first entry that contains a link to said first one of the plurality of page tables **["MLST" 78, Figure 3]**, said shadow page table **["Self-mapping Page Tables" coinciding in virtual-address space, Column 4, Lines 1-3]** comprising a second entry that corresponds to the first entry, said second entry containing a link to said shadow page table **["MLST" 80, Figure 3]** instead of a link to said first one of the plurality of page tables"

Harvey et al. do not disclose expressly, "an item of software uses said page table to perform a non-address-mapping action that depends on data that a characteristic that is present in said one of the plurality of page tables but not present in said first shadow page table".

Budd et al. disclose application software that performs a non-address-mapping action (comparing the stored "checksum" and the data) in paragraph 62.

Harvey et al. and Budd et al. are analogous art because they are from the same field of endeavor of memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Harvey et al. by including an application software that performs checksum calculation as taught by Budd et al. in paragraph 62.

The motivation for doing so would have been to detect the corruption before the actual I/O submission as expressly taught by Budd et al. in paragraph 62.

Therefore, it would have been obvious to combine Budd et al. with Harvey et al. for the benefit of early detection of data corruption to obtain the invention as specified in claim 19.

6. **Claims 2, 10 and 24** disclose, "access to said memory based on said address translation map applied to said virtual address results in violation of said policy, and wherein access to said memory based on said shadow page directory and said first shadow page table being applied to said virtual address does not result in violation of said policy". **In column 15, at lines 13-16, Harvey et al. recites, "This exception handler has been arranged in the illustrated embodiment to determine whether a true access violation has actually occurred",** which corresponds to the "policy" from the claim. **In column 15, at lines 26-31, Harvey et al. recites, "The handler**

compares the faulting reference with the shared/physical boundary to determine which of the two physical page frames identified by FIG. 3's registers 38 and 122 is the one that properly contains the page translation for that reference, and it fetches the proper entry by physical addressing." The "faulting reference" corresponds to the "virtual address results in violation" from the claim, and "fetching the proper entry by physical addressing" corresponds to the "virtual address does not result in violation" from the claim.

7. **Claim 3** discloses, "Each of the data pages is stored at a particular frame of a memory, wherein said page directory is stored at a first frame." **In figure 3,** Harvey et al. shows the "data page frames" which corresponds to the "data pages" from the claim, and the "top-level index" which corresponds to the "first frame" from the claim.

"Maintaining a copy of said page directory at a second frame different from said first frame." **In column 9, at lines 25-28, Harvey et al. recites, "The subtables located at some virtual-memory locations have different versions for different processes, and each is therefore materialized in different physical memory",** which means that the copies of the subtables are maintained in the different physical memory locations which corresponds to the "second frame different from said first frame" from the claim.

"Storing the shadow page directory at said first frame." **In figure 3,** the self-mapped TLST (96) is stored at the same page frame.

8. **Claim 4** discloses, "Page directory comprises a link to a first-sized page, said first-sized page comprising a plurality of second-sized pages." **In column 6, at lines 31 to 33, Harvey et al. recites, "An advantage of a multi-level page table is that it can manage large numbers of pages but requires little table space when the number of pages is small"**, which means that referring to **figure 3,** the "top-level index (76)" (corresponding to the "page directory" from the claim) links to the multiple "middle-level indexes (78, 80)" (corresponding to the "second-sized pages" from the claim).

"Creating a second shadow page table that comprises links to a said plurality of second sized pages, wherein said shadow page directory comprises a link to said second shadow page table." **In figure 3,** the "middle-level index" (corresponding to the "second shadow page table" from the claim) links to the "bottom-level index" (corresponding to the "second sized pages" from the claim), and the "top-level index" (corresponding to the "shadow page directory" from the claim) links to the "middle-level index" (corresponding to the "second shadow page table").

9. **Claim 6 and 16** disclose, "a plurality of page tables **["BLST" 94, Figure 3, Harvey et al.]** that contain links to said plurality of pages **["Byte within Page" 60, Figure 3, Harvey et al.]**".

"A page directory **["TLST" 76, Figure 3, Harvey et al.]** that contains links to said plurality of page tables, and wherein said shadow representation of said address translation data structure **["TLST" 96, Figure 3, Harvey et al.]** differs from said address translation data structure with respect to at least one link **[Link to "MLST" 80 instead of "MLST" 78, Figure 3, Harvey et al.]**"

10. **Claim 7** discloses, "each of the links contained in said page directory and said page tables contain one or more attributes, and wherein at least one link in said shadow representation differs from a corresponding link in said address translation data structure with respect to at least one attributes". **In column 4, at lines 14-15, Harvey et al. recites, "Whose contents are not in general identical to those of other constituents."** The "whose contents" refer to the contents in the "different physical-address location", and they correspond to the "attribute" from the claim.

11. **Claim 8** discloses, "each of the links in the page directory and page tables identifying one of the pages based on the physical location descriptor **[Link to physical "data page frames", Figure 3]**".

12. **Claim 9** discloses, "said shadow representation includes an alternative version of at least one of said page directory or one of said page tables, and wherein said alternative version is stored at a page having a different physical location descriptor from the page on which the alternative version is based". **In column 9, at lines 25-28,**

Harvey et al. recites, "Subtables located at some virtual-memory locations have different versions for different processes, and each is therefore materialized in different physical memory." The "different versions for different processes" correspond to the "alternative version" from the claims, and they are materialized in different physical memory.

13. **Claims 11 and 15** disclose, "defines a portion of memory as being inaccessible, wherein said map exposes writeable links to portions of said memory that define virtual address mappings, and wherein said representation of said map does not expose writeable links to portions of said memory that define virtual address mappings". **In column 15, at lines 12-16, Harvey et al. recites, "Invalid-access-exception handler, this exception handler has been arranged in the illustrated embodiment to determine whether a true access violation has actually occurred",** which corresponds to the "policy" from the claim. **In column 17, at lines 2-6, Harvey et al. recites, "Since this flag is encountered in the translation buffer during a translation that would yield a page frame containing a version of the top level subtable, the write operation does not occur."** When the flag (determines whether the memory is writable or not) is set, the operation is write-protected which means it is "read-only". The "translation buffer" contains the "shadow representation" from the claim, and it is "write-protected" ("does not expose writeable link").

14. **Claim 12** discloses, "the policy defines a portion of the memory as being readable but not writeable, and wherein the memory access control manager ensures that the shadow representation contains one or more attributes that mark the portion of memory as being read-only". **In column 17, at lines 2-6, Harvey et al. recites, "Since this flag is encountered in the translation buffer during a translation that would yield a page frame containing a version of the top level subtable, the write operation does not occur."** When the flag (determines whether the memory is writable or not) is set, the operation is write-protected which means it is "read-only". The "translation buffer" contains the "shadow representation" from the claim, and it is "write-protected" ("read-only") link.

15. **Claim 13** disclose, "the memory access control manager ensures that the shadow representation contains one or more attributes that mark as read-only those portions of the memory that store at least one of: (1) the address translation data structure; and (2) the shadow representation". **In column 17, at lines 1, Harvey et al. recites, "The illustrated embodiment write protects the top-level subtable."** The "top-level subtable" (76 from **figure 3**) corresponds to the "address translation structure" from the claim. Also, the self-mapped "top-level subtable (96) corresponds to the "shadow representation" from the claim.

16. **Claim 17** recites, "First link is a read/write link in said one of said tables, and wherein said shadow page differs from said one of said tables in that said shadow

page's representation said first link is marked read-only." **In column 17, at lines 2-6, Harvey et al. recites, "Since this flag is encountered in the translation buffer during a translation that would yield a page frame containing a version of the top level subtable, the write operation does not occur."** When the flag is set, the operation is write-protected which means it is "read-only". The "translation buffer" contains the "shadow page" from the claim, and it is "write-protected" ("read-only") link.

17. **Claim 18** recites, "Said shadow pages differs from said directory in that said shadow page contains a link to a table instead of a link to said first-sized page, wherein said table contains links to second-sized pages." **In figure 3,** the "middle-level index" (corresponding to the "shadow page" from the claim) links to the "bottom-level index" (corresponding to the "second-sized pages" from the claim), and the "top-level index" (corresponding to the "directory" from the claim) links to the "middle-level index" (corresponding to the "first-sized page").

18. **Claim 20** discloses, "the first of the plurality of page tables is stored at a first frame, wherein the shadow page table is stored at a second frame, and wherein the shadow page directory **[Self-mapped "TLST" 96, Figure 3, Harvey et al.]** differs from the page directory **["TLST" 76, Figure 3, Harvey et al.]** in the respect that a link in the page directory contains an identifier of said first frame **["MLST" 78, Figure 3, Harvey et al.]** and the corresponding link in the shadow page directory contains an identifier of said second frame **["MLST" 80, Figure 3, Harvey et al.]**".

19. **Claim 21** discloses, "Said shadow page table contains a link to a representation based on said first one of the pages instead of the link to the first one of the pages, said representation based on said first one of the pages being stored at a frame different from said first one of the pages." **In column 9, at lines 25-28, Harvey et al. recites, "The subtables located at some virtual-memory locations have different versions for different processes, and each is therefore materialized in different physical memory",** which means that the copies of the subtables are maintained in the different physical memory locations which corresponds to the "different frame" from the claim, and the "subtables" corresponds to the "shadow page table" from the claim.

20. **Claim 22** recites, "First one of the plurality of pages stores either the page directory or said first one of the plurality of page tables." The "plurality of pages" corresponds to the "TLST and MLST page frames" in **figure 3**. The "page directory" corresponds to the "top-level index" in **figure 3**, and the "page tables" corresponds to the "middle-level index" in **figure 3.**

21. **Claim 23** recites, "First one of the plurality of page tables contains a link that specifies said first one of the plurality of pages as being readable and writeable, and wherein the corresponding link in said shadow page table specifies said first one of the plurality of pages as being only readable." **In column 17, at lines 2-6, Harvey et al. recites, "Since this flag is encountered in the translation buffer during a**

translation that would yield a page frame containing a version of the top level subtable, the write operation does not occur." When the flag is set, the operation is write-protected which means it is "read-only". The "translation buffer" contains the "shadow page table" from the claim, and it is "write-protected" ("read-only") link.

Relevant Art Cited by the Examiner

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See MPEP 707.05(C).

The following reference teaches a **self-mapping virtual memory** that corresponds to multiple physical memory locations.

Non-Patent Literature	**Figures**
Harvey et al., Extending Open VMS for 64-Bit Addressable Virtual Memory, *Digital Technical Journal,* vol. 8, No. 2 (1996).	3 and 4

Conclusion

A. Claims Rejected in the Application

Per the instant office action, claim 1-24 have received a second action on the merits and are subject of a second action final.

B. Direction of Future Correspondences

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae U. Yu whose telephone number is 571-272-1133. The examiner can normally be reached on M-F 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 9, 2006

Jae Un Yu
Art Unit 2185

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DONALD SPARKS
SUPERVISORY PATENT EXAMINER